

國立中山大學九十三年度碩士班招生考試試題

科目：計算機結構（資訊工程學系碩士班）

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If some questions are unclear or not well defined to you, you can make your own assumptions and state them clearly in the answer sheet.

I. 選擇題：Please choose the most appropriate answer (one only) to each following question. (30%)

1. Which of the following metric will not benefit from the forwarding technique (a) program instruction count (b) execution time (c) data hazard stall (d) effective CPI.
2. Considering a direct-mapped cache with 64 blocks and block size of 16 bytes, what block number does memory address $(256)_{10}$ map to (a) 4 (b) 16 (c) 64 (d) 256
3. Which of the following style of instruction sets is most likely to achieve smallest instruction count while compiling a program? (a) accumulator (b) load-store (c) stack (d) memory-memory
4. How many bits of ROM is required to implement a Moore finite-state machine with 8 states, 2 input and 3 output control signals? (a) 48 (b) 60 (c) 96 (d) 192
5. To get a speed up of 5 from 20 processors, which number is closest to the minimum percentage of the original program that has to be sequential? (a) 5% (b) 10% (c) 16% (d) 80%
6. What is the main advantage by adding some complex instructions into the existed instructions sets? (a) reduced CPI (b) less instruction count (c) faster clock cycle (d) increased MIPS.
7. Which of the following RISC addressing model will involve the memory operation? (a) Base addressing (b) Register addressing (c) PC-relative addressing (d) immediately addressing
8. Which of the following floating point number represented in IEEE 754 standard (1-bit for sign, 8-bit for exponent) is the largest? (a) 0 11111111 100000000000000000000000 (b) 0 01000000 100000000000000000000000 (c) 1 11000000 100000000000000000000000 (d) 0 10000000 000000000000000000000000
9. Which of the following statement about computer arithmetic is correct? (a) Basic Booth's algorithm can always improve the multiplication speed (b) The addition of two floating point numbers won't overflow (c) The subtraction of two two's complement numbers won't overflow (d) The floating-point addition is not associative.
10. What's not the advantage of the addition of second level cache? (a) reduced miss penalty (b) reduced miss rate of the first level cache (c) reduced effective CPI (d) reduced program's execution time
11. The compiler technique can help improving many metrics except (a) average CPI (b) clock frequency (c) miss rate (d) control hazard
12. Which of the following feature is not typical for the RISC machine? (a) powerful instruction set (b) small CPI (c) limited addressing mode (d) simple hardware architecture
13. Which of the following statement about the use of larger block size is correct? (a) It can always reduce the miss rate. (b) It can reduce the miss rate because of the temporal locality of the program. (c) It can reduce compulsory misses. (d) It can reduce the miss penalty.

14. By increasing the pipelined depth of the machine, (a) the execution time can always be reduced (b) the chance of hazard becomes smaller (c) the average CPI may increase (d) None of the above are correct.
15. Which of the statements about the single cycle, multicycle and pipelined implementation of MIPS machine is correct (a) Single cycle machine requires least amount of hardware (b) Pipelined machine has the smallest effective CPI (c) Multicycle machine requires least amount of hardware (d) The clock frequency of the multicycle machine is slowest.

II. Computer Datapath

Fig. 1 shows the complete datapath of the multi-cycle implementation of MIPS processor.

1. (4%) Describe the function of the following segment of the program. (\$zero is one MIPS register and always 0. Register \$a1 equals 10 initially.)

```

        add      $t0, $zero, $zero
loop1:  add      $t1, $t0, $t0
        add      $t1, $t1, $t1
        add      $t2, $a0, $t1
        sw       $zero, $0($t2)
        addi     $t0, $t0, 1
        slt     $t3, $t0, $a1
        bne     $t3, $zero, loop1
    
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2. (8%) Evaluate the CPI of the individual instruction in the above program, and also calculate the overall CPI for running the entire program.
3. (6%) Let's suppose the overflow of ALU operation will lead to an exception. When this exception occurs, the machine will jump to special interrupt routine services at 0x000C, and the old PC will be written to a specific register \$k1. Discuss how to modify the datapath to support this exception's behavior.
4. (6%) If we pipeline the datapath shown in Fig.1 to achieve a five-stage pipelined MIPS, some pipelining hazard may occur while running the above program. Find out what hazards will occur and how many cycles the machine will stall related to the execution of the instruction **bne \$t3, \$zero, loop1**. (Assume no data forwarding mechanism is used, and the register read/write can happen in the same cycle.)
5. (6%) One way to cope up with the hazard is to use **branch delay slot**. Explain this concept and illustrate how to apply it to the program shown as above.

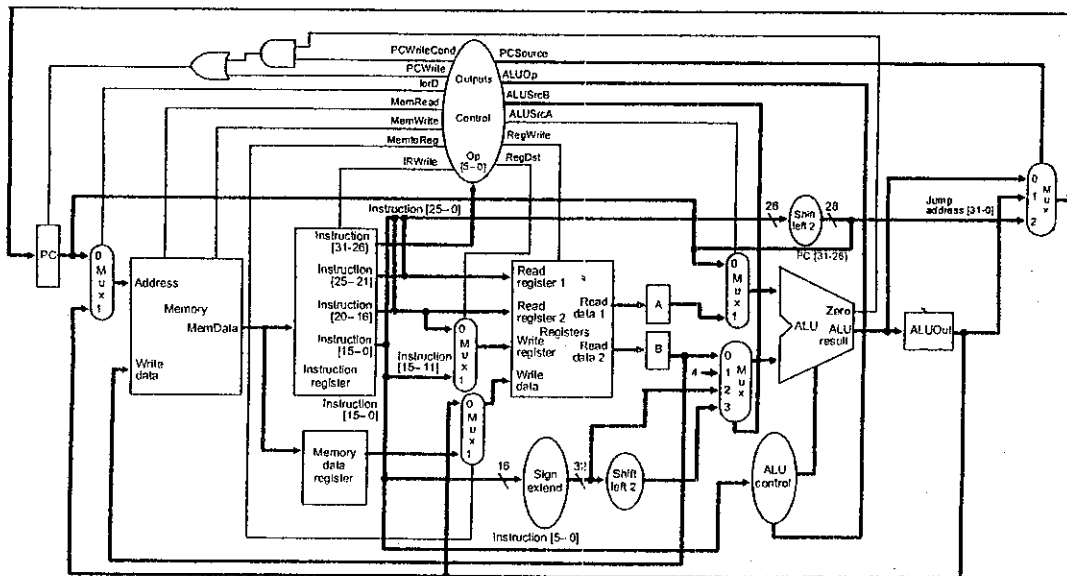


Fig. 1

III. Cache

Suppose the gcc program is run on some 200 MHz RISC machine for a two-way associated unified cache with 64-KB of data and four-word block. This miss rate of instruction and data memory access is 2% and 6% respectively. The CPI of the machine is 2 when there is no memory stall. The miss penalty is 40 cycles for all misses. The instruction mix of the gcc program is 22% load, 8% store, 50% R-type, 18% branch and 2% jump instructions. The instruction length of this processor is 32-bit wide.

1. (8%) Draw the cache organization and calculate the overall size of the cache including the tag and the valid bit.
2. (8%) Calculate the MIPS of this machine for running the gcc program.
3. (3%) In some cache organization, some *dirty bit* will be used. Discuss the purpose of the use of *dirty bit*.
4. (6%) Virtual memory can be regarded as another level of the memory hierarchy. Compare the virtual memory and data cache from the following aspects: block placement scheme, block replacement strategies and write policy.

IV. Computer arithmetic:

1. (5%) Draw the gate-level implementation of a full adder.
2. (10%) Draw the detailed architecture of a simple ALU as shown in Fig. 2 capable of performing 4-bit two's complement addition and subtraction. When *op* equals 1, it will perform the operation of (A+B) while *op* equals 0, it will perform the operation of (A-B). This ALU will set the flag *f_over* (=1) when overflow occurs. The other flag *f_comp* will be set when two numbers are equal (i.e. A=B).

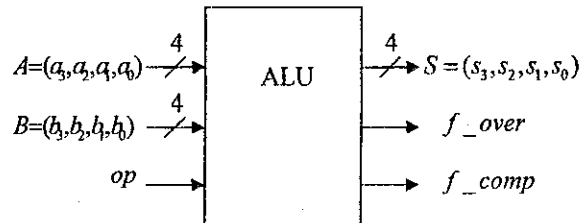


Fig. 2

1. (5%) Consider a system with four processes P_1 through P_4 and five allocatable resources R_1 through R_5 . The current allocation and maximum needs are as follows:

	Allocated	Maximum	Available
P_1	1 0 2 1 1	1 1 2 1 2	0 0 x 1 1
P_2	2 0 1 1 0	2 2 2 1 0	
P_3	1 1 0 1 0	2 1 3 1 0	
P_4	1 1 1 1 0	1 1 2 2 1	

What is the smallest value of x for which this is a safe state?

2. (9% total; 3% each subquestion) Consider the following page reference string:

1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 2, 3, 7, 6, 3, 2, 1, 2, 3, 6.

How many page faults would occur for the following replacement algorithms, assuming one, two, three, four, five, six, or seven frames? Remember that all frames are initially empty, so your first unique pages will all cost one fault each.

- LRU replacement
 - FIFO replacement
 - Optimal replacement
3. (18% total; 3% each subquestion) Suppose that a disk drive has 1000 cylinders, numbered from 0 to 999. The drive is currently serving a request at cylinder 200, and the previous request was at cylinder 125. The queue of pending requests, in FIFO order, is

50, 500, 250, 800, 350, 550, 400, 600, 150.

Starting from the current head position, what is the total distance (in cylinders) that the disk arm moves to satisfy all the pending requests for each of the following disk scheduling algorithms?

- FCFS
 - SSTF
 - SCAN
 - LOOK
 - C-SCAN
 - C-LOOK
4. (10% total; 2% each subquestion) Measurements of a certain system have shown that the average process runs for a time T before blocking on I/O. A process switch requires a time S , which is effectively wasted (overhead). For round-robin scheduling with quantum Q , give a formula for the CPU efficiency for each of the following:
- $Q = \infty$
 - $Q > T$
 - $S < Q < T$
 - $Q = S$
 - Q nearly 0

5. (8% total; 4% each subquestion) Consider the following preemptive priority-scheduling algorithm based on dynamically changing priorities. Larger priority numbers imply higher priority. When a process is waiting for the CPU (in the ready queue but not running), its priority changes at a rate α ; when it is running, its priority changes at a rate β . All processes are given a priority of 0 when they enter the ready queue. The parameters α and β can be set to give many different scheduling algorithms.

- What is the algorithm that results from $\beta > \alpha > 0$?
- What is the algorithm that results from $\alpha < \beta < 0$?

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6. (10 %) Multiple choice.

(a) Choose ALL the correct statements.

(A) A queue is a last-in, first-out list.

(B) For deletion, a priority queue implemented as an ordered linked list takes $\Theta(1)$ time.

(C) For the implementation of a recursive program, a stack mechanism is maintained by a programming system that supports recursion.

(D) For the implementation of a sparse matrix, an array is more efficient than a linked list.

(E) None of the above.

(b) Choose ALL the correct statements for a graph G with n vertices and e edges.

(A) The time complexity to find a cycle using depth-first search is $O(e \log n)$.

(B) The time complexity of breadth-first search for the adjacency list representation is $O((n+e) \log n)$.

(C) For the graph traversal, depth-first search is more efficient than breadth-first search.

(D) The adjacency list representation is more efficient than the adjacency matrix representation for the graph operations of both depth-first search and breadth-first search.

(E) None of the above.

7. (10 %) Suppose that the preorder sequence is EBCAFDG and the inorder sequence is CBFAEGD for the same binary tree.

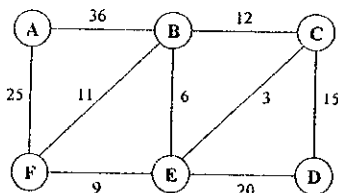
(a) Draw the binary tree.

(b) Write out the postorder sequence for the binary tree.

8. (10 %) Construct the minimum cost spanning tree for the following weighted graph.

(a) Write out each weight of the edges added to the tree in the sequence of applying Kruskal's algorithm.

(b) Draw the minimum cost spanning tree.



9. (10 %) Consider the following alphabet and frequency table.

(a) Draw the Huffman coding tree.

(b) Write out the Huffman code for the message EADGF.

Character	A	B	C	D	E	F	G
Frequency	18	30	9	12	16	2	15

10. (10 %) Consider a sequence of keys as follows.

11	36	49	2	25	32	22	16
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Draw the corresponding trees by inserting the keys in the given order into an initially empty tree of the following structure.

(a) AVL tree.

(b) 2-3 tree.

1. [10%] Determine the number of positive integer solutions of

$$x_1 + x_2 + x_3 + x_4 + x_5 = 45$$

where x_i must be exactly divided by 3 for $i = 1, 2, 3, 4,$ and 5 .

2. [10%] If $\binom{n}{r} = \frac{n!}{r!(n-r)!}$, $0 \leq r \leq n$, and n is an even integer, then

$$2\binom{n}{0} + \binom{n}{1} + 2\binom{n}{2} + \binom{n}{3} + 2\binom{n}{4} + \binom{n}{5} + \dots + 2\binom{n}{n-2} + \binom{n}{n-1} + 2\binom{n}{n} = ?$$

3. Let $S(m, n)$ be a Stirling number of the second kind where m, n are integers and $1 < n \leq m$.

(a) [5%] $S(8, 3) = ?$

(b) [5%] If $S(m, n-1) = a$ and $S(m, n) = b$, then $S(m+1, n) = ?$

4. Let A be a set and $|A| = n > 0$.

(a) [5%] How many relations on A are not symmetric?

(b) [5%] How many relations on A are anti-symmetric?

5. (a) [5%] Let $G = (V, E)$ be a connected planar graph or multigraph with $|V| = 1500$ and $|E| = 3000$. What is the number of regions in the plane determined by a planar embedding (or, depiction) of G .

(b) [5%] For $n \geq 3$, how many different Hamilton cycles are there in the complete graph K_n ?

6. [15%] Find an integer m such that $0 < m < 23 \cdot 29 \cdot 31$ and

$$\begin{cases} m \equiv 1 \pmod{23} \\ m \equiv 0 \pmod{29} \\ m \equiv 2 \pmod{31} \end{cases}$$

by the Chinese Remainder Theorem.

7. Solve the following recurrence relations:

(a) [5%] $a_n - 6a_{n-1} + 9a_{n-2} = 0$, $n \geq 2$, $a_0 = 5$, $a_1 = 12$.

(b) [5%] $a_{n+1} - 2a_n = 2^n$, $n \geq 0$, $a_0 = 1$.

(c) [10%] $a_{n+2}^2 - 5a_{n+1}^2 + 6a_n^2 = 7n$, $n \geq 0$, $a_0 = 1$, $a_1 = 1$.

8. [15%] Let $M = (S, I, O, v, w)$ be a finite state machine, where $S = \{a, b, c, d, e, f\}$ is the set of states; $I = \{0, 1\}$ is the input alphabet for M ; $O = \{0, 1\}$ is the output alphabet for M ; $v: S \times I \rightarrow S$ is the next state function; and $w: S \times I \rightarrow O$ is the output function defined as follows:

	v		w	
	0	1	0	1
a	d	c	0	1
b	e	b	1	0
c	b	d	0	0
d	e	c	0	0
e	b	e	1	0
f	a	f	1	0

Which states are equivalent after performing the minimization process on M ?