科目名稱:離散數學【資工系碩士班甲組】

#### -作答注意事項-

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科目名稱:離散數學【資工系碩士班甲組】

題號: 434004

※本科目依簡章規定「不可以」使用計算機(問答申論題)

共1頁第1頁

There are 8 problems in this test. Note that you should write down detailed steps for the solution to each problem; otherwise, no credits for that problem will be given.

1. Consider the following program segment (written in pseudocode):

- (a) [10%] How many times is the print statement of the third line executed?
- (b) [10%] Replace i in the second line by  $i^2$  and answer the question in part (a).
- 2. [10%] If  $n \in \mathbb{Z}^+$  and n is composite, then there is a prime p such that p|n.
- 3. (a) [10%] Prove that if 169 integers are selected from  $\{1, 2, 3, \dots, 336\}$ , then the selection must include two integers x, y, where x|y or y|x.
  - (b) [10%] Write a statement that generalizes the results of part (a).
- 4. [10%] Let  $\Sigma = \{v, w, x, y, z\}$  and  $A = \bigcup_{n=1}^{8} \Sigma^{n}$ . How many strings in A have xy as a proper prefix?
- 5. [10%] If a fair die is rolled 11 times, what is the probability that the sum of the rolls is 35?
- 6. [10%] Solve the recurrence relation

$$a_{n+2} - 4a_{n+1} + 3a_n = -360, n \ge 0, a_0 = 3000, a_0 = 3300.$$

- 7. [10%] Find [23]<sup>-1</sup> in  $Z_{82}$  by Euclidean algorithm.
- 8. [10%] How many integer solutions are there of the equation  $c_1 + c_2 + c_3 + c_4 + c_5 =$  37 if  $0 \le c_i$  for all  $1 \le c_i \le 5$ ?

科目名稱:作業系統與資料結構【資工系碩士班甲組】

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科目名稱:作業系統與資料結構【資工系碩士班甲組】 ※本科目依簡章規定「不可以」使用計算機(問答申論題)

題號: 434003 共2頁第1頁

INSTRUCTIONS: If any question is unclear or you believe some assumptions need to be made, state your assumptions clearly at the beginning of your answer.

1. (10%) What would be the output of the following C program? (Note that the line numbers are for reference only.)

```
#include <stdio.h>
2 #include <unistd.h>
3 #include <sys/types.h>
4 #include <sys/wait.h>
5 int main()
6 {
       int fd[2];
       pipe(fd);
       pid_t pid = fork();
       if (pid > 0) {
10
           close(fd[1]);
11
           close(0):
12
           dup(fd[0]);
13
           close(fd[0]);
14
           int status;
           waitpid(-1, &status, 0);
16
           char buf [128]:
17
           int n = scanf("%s", buf);
18
           printf("%d:%s\n", n, buf);
19
20
       else if (pid == 0) {
21
           close(fd[0]);
22
           close(1);
23
           dup(fd[1]);
24
           close(fd[1]);
25
           execl("/bin/echo", "echo", "hello", "world!", (void*) 0);
26
27
       7
28
       else {
29
           return 1;
30
31
       return 0:
32 }
```

2. (10%) Suppose that a disk drive has 1001 cylinders, numbered from 0 to 1000. The drive is currently serving a request at cylinder 175, and the previous request was at cylinder 125. The queue of pending requests, in FIFO order, is

50, 500, 225, 825, 350, 550, 400, 600, 100.

Starting from the current head position, what is the *total distance* (in cylinders) that the disk arm moves to satisfy all the pending requests for each of the following disk scheduling algorithms?

- (a) (2%) FCFS
- (b) (2%) LOOK
- (c) (2%) C-LOOK
- (d) (2%) SCAN
- (e) (2%) C-SCAN
- 3. (10%) A computer whose processes have 2048 pages in their address spaces keeps its page tables in memory. The overhead required for reading a word from the page table is 500 nsec. To reduce this overhead, the computer has a TLB, which holds 32 (page, frame) pairs and can do a lookup in 50 nsec. What hit rate is needed to reduce the mean overhead to 150 nsec or less, assuming that TLB is looked up first before the page table is read?

科目名稱:作業系統與資料結構【資工系碩士班甲組】 ※本科目依簡章規定「不可以」使用計算機(問答申論題)

題號: 434003 共2頁第2頁

- 4. (10%) Given a UNIX *i*-node with sixteen direct blocks and four levels of indirect blocks (i.e., a single, a double, a triple, and a quadruple) and assuming that the sizes of a pointer and a block are, respectively, 8 bytes and 8 Kbytes, answer the following questions.
  - (a) (5%) What would be the size of the smallest file allowed in bytes?
  - (b) (5%) What would be the size of the largest file allowed in bytes?
- 5. (10%) Consider the two-dimensional array a:

```
double a[][] = new double[400][400];
```

where each double occupies 8 bytes and a [0] [0] is at location 400, in a paged system with pages of size 400 bytes. A small process is in page 0 (locations 0 to 399) for manipulating the matrix; thus, every instruction fetch will be from page 0. For three page frames, how many page faults are generated by the following array initialization loops, using LRU replacement and assuming (1) page frame 0 has the process in it, (2) the other two are initially empty, and (3) the array is stored in memory row-major.

(a) (5%)

```
for (int j = 0; j < 400; j++)
for (int i = 0; i < 400; i++)
a[i][j] = 0;
```

(b) (5%)

- 6. (10%) What are printed by each of the following program segments?
  - (a) (5%)

```
int a=48; printf("%d \n", (a&(-a)) >>2);
```

(b) (5%)

```
int a=68, b=34, c=25;
printf("%d %d \n",a^a^a^b^a, (a^b^c^b^a^c^a)+17); //^:XOR
```

- 7. (10%) Suppose that the preorder sequence of a binary tree is ABCDEFGH, and the inorder sequence is ABDAFGHE. What is the postorder sequence of the binary tree?
- 8. (15%) In the hash method, suppose that a rehash function  $h_i(x)=(5i+x) \mod 13$  is applied sequentially when a new element is inserted into the hash table, but a hash collision occurs. In other words,  $h_1()$  is applied for the first time;  $h_2()$  is applied if a hash collision occurs;  $h_3()$  is applied if a hash collision occurs again; and so on. What is the content of the hash table after the elements 35, 22, 9, 24, 16, 19, 3, are inserted sequentially into an empty hash table of size 13, indexed as 0 through 12?
- 9. (a) (5%) Please give the definition of an AVL binary search tree.
  - (b) (5%) Assume that the initial AVL tree is empty. Please draw the AVL tree after the numbers 8, 9, 6, 3 and 2 are inserted into the tree sequentially.
  - (c) (5%) Please draw the AVL tree after the number 5 is inserted into the above AVL obtained in (b).

科目名稱:工程數學【資工系碩士班乙組】

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#### 科目名稱:工程數學【資工系碩士班乙組】

題號:434002

※本科目依簡章規定「不可以」使用計算機(問答申論題)

共1頁第1頁

1. (15%) The following matrix describes a system of linear equations in five unknowns: v, w, x, y, z. What is the general solution to this system?

$$\begin{bmatrix} 1 & 5 & 0 & 2 & -2 & 4 \\ 0 & 1 & 0 & 0 & 4 & 8 \\ 0 & 0 & 0 & 1 & 7 & -2 \end{bmatrix}$$

2. (15%) Consider the matrix

$$A = \begin{bmatrix} 3 & 0 & 0 \\ 0 & 2 & 1 \\ 0 & 1 & 2 \end{bmatrix}$$

- 2.1 (10%) Find the characteristic polynomial of A.
- 2.2 (5%) Find the eigenvalues for A.

3. (20%) Find the impulse and step responses of a system with transfer function.

$$H(s) = \frac{2S^2 - 10s + 1}{S^2 + 3s + 2}$$

4. (15%) A signal x(t) is periodic with period  $T_0 = 8$ . Therefore, it can be reproduced as a Fourier series:

$$x(t) = \sum_{k=-\infty}^{\infty} a_k e^{j\left(\frac{2\pi}{8}\right)kt}$$

The Fourier series coefficients for this representation of a particular signal x(t) are given by the integral

$$a_k = \frac{1}{8} \int_{-4}^{0} (4+t)e^{-j\left(\frac{2\pi}{8}\right)kt} dt$$

- 4.1 (5%) In the integral expression for  $a_k$  above, the integrand and the limits define the signal x(t). Determine an equation for x(t) that is valid over one period.
- 4.2 (5%) Using the result from part 4.1, draw a plot of x(t) over the range of  $-8 \le t \le 8$  seconds.
- 4.3 (5%) Determine the DC value of x(t).
- 5. (20%) Find a particular solution of

$$y''' - 4y' = t + 3\cos t + e^{-2t}$$

6. (15%) Find the solution of the given initial value by using Laplace transform and inverse Laplace transform.

$$y'' + 4y = 3\sin(2t)$$
,  $y(0) = 2$ ,  $y'(0) = -1$ 

科目名稱:計算機結構【資工系碩士班甲組、乙組】

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科目名稱:計算機結構【資工系碩士班甲組、乙組】 題號:434001 ※本科目依簡章規定「不可以」使用計算機(問答申論題) 共2頁第1頁

- 1. All the following questions are multiple-choice questions. <u>Please explain your reasons for the choices, which you don't select.</u> (10%)
  - 1.1 (2%) A computer has 128MB of memory. Each word in the computer is eight bytes. How many bits at least are needed to address any single word in memory? (a) 8 bits (b) 16 bits (c) 24 bits (d) 32 bits
  - 1.2 (2%) In modern computer architectures, TLB is usually involved to improve the efficiency of the memory hierarchy. If we meet a situation of TLB miss, what is the following description true?
    - (a) The data requested by the CPU must be not in the cache.
    - (b) The data requested by the CPU must be not in the main memory.
    - (c) The CPU is failed to get the physical address of the required data.
    - (d) The CPU must send a request to access the main memory immediately.
  - 1.3 (2%) To solve the cache coherence problem, Snoopy protocol is the simplest. Regarding the Snoopy coherence protocol, what is the following description true?
    - (a) Any CPU should invalidate the cache block if it receives a write miss signal to the data in the local cache block from the bus.
    - (b) Any CPU should invalidate the cache block if it receives a read miss signal to the data in the local cache block from the bus.
    - (c) The Snoopy coherence protocol is an atomic operation.
    - (d) The Snoopy coherence protocol is proper to apply to a single-core system.
  - 1.4 (2%) Regarding the cache miss, what is the following description true?
    - (a) Compulsory miss indicates that the cache cannot contain all blocks required for the execution.
    - (b) Coherence miss only happens in multi-core systems.
    - (c) The miss rate will go down while the block size is made very large.
    - (d) Increasing the associativity decreases miss rate due to lower compulsory miss.
  - 1.5 (2%) Regarding the cache design, what is the following description true?
    - (a) With the criteria of the identical entries, we need more tag bits in a multi-word cache than in set-accusative cache.
    - (b) Through interchanging the loops in a code, the cache miss rate cannot be degraded.
    - (c) Through the way prediction technique, the miss penalty during the cache access can be reduced.
    - (d) If we pipeline the cache access, the cache bandwidth can be improved.
- 2. (30%) Suppose we have a processor with a base CPI of 1.0, assuming all reference hit in the primary cache, and a clock rate of 5GHz. Assume a main memory access time of 100 ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 2%.
  - 2.1 (10%) What is the CPI if this single-core processor only has one level of cache?
  - 2.2 (20%) To speed up the process, we increase the CPU cores from 1-core CPU to 2-core CPU and retain other design settings. We assume 60% of instructions must be executed sequentially. Please estimate the speedup ratio by using the new architecture.
- 3. (20%) Assume a GPU architecture that contains 10 SIMD processors. Each SIMD instruction has a width of 32 and each SIMD processor contains 8 lanes for single-precision arithmetic and load/store instructions, meaning that each non-diverged SIMD instruction can produce 32 results every 4 cycles. Assume a kernel that has divergent branches that cause on average 80% of threads to be

科目名稱:計算機結構【資工系碩士班甲組、乙組】 ※本科目依簡章規定「不可以」使用計算機(問答申論題)

題號: 434001 共2頁第2頁

active. Assume that 70% of all SIMD instructions executed are single-precision arithmetic and 20% are load/store. Since not all memory latencies are covered, assume an average SIMD instruction issue rate of 0.85. Assume that the GPU has a clock speed of 1.5 GHz. Please compute the throughput, in GFLOP/sec, for this kernel on this GPU.

4. (40%) You are a system engineer. Today, you need to design a memory hierarchical system, including one CPU, one or two-level cache, one main memory, and one hard disk. Currently, you have the following design policies for the cache-level design.

**Policy 1:** With only L1 cache by using 2-way associativity

Policy 2: With direct mapping L1 cache and 2-way associative L2 cache

Policy 3: With 2-way associative L1 and L2 caches

Assume that there is one embedded TLB in each cache level and one embedded page table in the main memory (*i.e.*, we do not need extra memory to store the TLB and page table). On the other hand, the specifications of this memory hierarchical system are

- This is a 32-bit machine.
- The base CPI is 1.0 and the clock rate is 5GHz.
- Each cache block is a single-word block.
- The L1 cache can contain 8KB data.
- The L2 cache can contain 16KB data.
- $\blacksquare$  The page size is  $2^{12}$  bytes.
- In the TLB and page table, we need to involve an extra one dirty bit to implement the write-back policy; one reference bit to approximate the LRU replacement policy; one valid bit to judge the data hit/miss.
- The number of the TLB entries in L1 and L2 caches are 10 and 20 respectively. Besides, the number of entries in the page table is 30. To reduce the miss rate, the fully associative policy is adopted to implement the TLB and page table.
- 4.1 (10%) Please determine the number of bits required in the page table, TLB in the L1 cache, and TLB in the L2 cache.
- 4.2 (10%) Please determine the number of bits required if
  - a. (5%) L1 cache is implemented by using 2-way associative mapping strategy.
  - b. (5%) L2 cache is implemented by using 2-way associative mapping strategy.
- 4.3 (20%) Without considering the data transferring time, we assume the access time of L2 cache is 5 ns including all the miss handling; the access time of the main memory is 100 ns including all the miss handling; the access time of the hard disk is 1 us including all the miss handling. According to the data transference time between each memory level, we ignore the data transference time between the L1 and L2 cache and the data transference time between the main memory and the lowest level cache and disk are both 50 ns including all the miss handling. In this system, the TLB will be located at the lowest level cache. When a data request comes, the TLB must be accessed first. If the TLB miss happens, we need to spend 10ns to handle the TLB-miss exception. When we adopt direct mapping strategy, the miss rate of the L1 cache and the embedded TLB are both 2%; the miss rate of the L2 cache and the embedded TLB are both 0.5%. If the 2-way mapping strategy is applied, the miss rate of the L1 cache and the embedded TLB are both 1%; the miss rate of the L2 cache and the embedded TLB are both 0.1%. At last, the miss rate of the main memory is 0.1%. During manufacturing, we need to spend 0.01 USD to handle one bit in each kind of memory. Please provide a design suggestion, including how many cache level you suggest and what kind of mapping strategy for each cache level you suggest, to your customer by considering the system performance and the manufacturing simultaneously cost.

科目名稱:離散數學與演算法【資工系資安碩班碩士班】

### 一作答注意事項-

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- 答案卷限用藍、黑色筆(含鉛筆)書寫、繪圖或標示,可攜帶橡皮擦、無色透明無文字墊板、尺規、修正液(帶)、手錶(未附計算器者)。每人每節限使用一份答案卷,不得另攜帶紙張,請衡酌作答。
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- 可否使用計算機請依試題資訊內標註為準,如「可以」使用,廠牌、功能不拘,唯不得攜帶具有通訊、記憶或收發等功能或其他有礙試場安寧、考試公平之各類器材、物品(如鬧鈴、行動電話、電子字典等)入場。
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- 試題採雙面列印,考生應注意試題頁數確實作答。
- 違規者依本校招生考試試場規則及違規處理辦法處理。

科目名稱:離散數學與演算法【資工系資安碩班碩士班】 ※本科目依簡章規定「不可以」使用計算機(問答申論題)

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There are 8 problems in this test. Note that you should write down detailed steps for the solution to each problem; otherwise, no credits for that problem will be given.

1. Prove each of the following for all  $n \ge 1$  by the Principle of Mathematical Induction.

(a)[10%]  $1 \cdot 3 + 2 \cdot 4 + 3 \cdot 5 + \dots + n(n+2) = \frac{n(n+1)(2n+7)}{6}$ . (b)[10%]  $\sum_{i=1}^{n} \frac{1}{i(i+1)} = \frac{n}{n+1}$ .

- 2. [10%] Prove that there are infinitely many primes.
- 3. (a)[10%] Show that if any 19 integers are selected from the set S = {1, 2, ..., 35}, there are at least two whose sum is 36.

  (b)[10%] Write a statement that generalizes the results of part (a).
- 4. [10%] Given an alphabet  $\Sigma$ , is there a language  $A \subseteq \Sigma^*$  where  $A^* = A$ ?
- 5. [10%] Find the generating function for the number of integer solutions to the equation  $c_1 + c_2 + c_3 + c_4 = 30$ , where  $-3 \le c_1, -2 \le c_2, -6 \le c_3 \le 6$ ,  $0 \le c_4$ .
- 6. (Algorithm points) [10%] Find  $[37]^{-1}$  in  $Z_{66}$  by Euclidean algorithm.
- 7. (Algorithm points) [10%] Please express quicksort algorithm and analyze its time complexity in detail.
- 8. (Algorithm points) [10%] Please express the construction of Huffman coding and analyze its time complexity in detail.

科目名稱:作業系統【資工系資安碩班碩士班】

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科目名稱:作業系統【資工系資安碩班碩士班】

**題號:485001** 共1頁第1頁

※本科目依簡章規定「不可以」使用計算機(問答申論題)

1. [Process: 20%]

- (1) Except for the process state, what are the six components in a process control block? (6%)
- (2) Please define interrupt latency and dispatch latency. (4%)
- (3) As compared with processes, will or will not context switching among multiple threads incur less overhead? Why or why not? (4%)
- (4) According to POSIX threads, what are the three procedures involved in a mutex and how to use them? (6%)

2. [Memory: 20%]

- (1) How do the first-fit, best-fit, and worst-fit methods work for memory allocation? (6%)
- (2) Why can virtual memory speed up process creation? (4%)
- (3) When using demand paging, what problem will occur in an inverted page table? How to solve that problem? (4%)
- (4) In case of a page fault, what are the six steps for the operating system to handle it? (6%)

3. [File and I/O: 20%]

- (1) What are the four major pieces of information associated with an open file? (4%)
- (2) Explain the six common types of access for a file. (6%)
- (3) What is the difference between physical and logical formatting of a disk? (4%)
- (4) What are the four typical registers associated with an I/O port? What are their functions? (4%)
- (5) What is a maskable interrupt? (2%)

4. [Threats: 20%]

- (1) What are phishing and dumpster diving? (4%)
- (2) Please give two OS-based solutions to the stack & buffer overflow problem. (4%)
- (3) How do parasitic and memory viruses work? (4%)
- (4) What is a worm? Please explain the two components of a worm. (6%)
- (5) What is session hijacking? (2%)

5. [Cryptography and Security: 20%]

- (1) How does one-way HMAC (hash-based message authentication code) key chain work? (7%)
- (2) Please give the five steps for a server and a client to generate a shared 48-byte master secret in SSL (secure sockets layer). (5%)
- (3) What is the difference between signature-based detection and anomaly detection? (4%)
- (4) Please give two vulnerabilities of a firewall. (4%)