國立中山大學107學年度碩士暨碩士專班招生考試試題

科目名稱：計算機結構【資工系碩士班甲組、乙組】　　題號：434001

※本科目依簡章規定「不可以」使用計算機(問答申論題)　　

1. (10% total) You are designing a processor for an IoT embedded system. Based on the analysis of the monitoring software, the instructions listed in Table 1 show the specified latencies.

Table 1.

Instructions	Frequency	Latency
load	10%	7 cycles
store	15%	10 cycles
branch	15%	4 cycles
add	55%	4 cycles
divide	5%	5 cycles

1.1 (2%) What is the CPI of your processor on this mix of instructions?

1.2 (2%) Based on your design, if you could halve the cycle latency of any single category of instruction, but at the cost of increasing the cycle time by 20%. Should you make this change, and if so, what category of instruction should you speed up? (load, store, branch, add, or divide)

1.3 (3%) What is the CPI of your new design?

1.4 (3%) What is the speedup of your revised design over the original one, rounded to the nearest tenth?

2. (15% total) The standard pipeline has five stages: fetch (F), decode (D), execute (X), memory (M), and writeback (W). Consider the following **four-stage** pipelines, formed by combining two stages of the classic five-stage pipeline.

2.1 (3%) What specific **positive** impact would combining the "D" and "X" stages have on **CPI**?

2.2 (3%) What specific **positive** impact would combining the "X" and "M" stages have on **CPI**?

2.3 (3%) What specific **positive** might combining the "M" and "W" stages have on the **clock frequency** of the pipeline?

2.4 (3%) What specific impact would combining the "F" and "D" stages have on the implementation of branch prediction?

2.5 (3%) If a single-cycle datapath with delay of n nanoseconds is converted into a pipelined datapath with p stages, the clock period will be longer (slower) than n/p nanoseconds. Give two reasons for this.

3. (10% total) Please answer the following questions:

3.1 (2%) What do VLIW, superscalar execution, and array processing concepts have in common?

3.2 (4%) Provide two reasons why a VLIW microarchitecture is simpler than a "same-width" superscalar microarchitecture?

3.3 (4%) Provide two reasons why a superscalar microarchitecture could provide higher performance than a "same-width" VLIW microarchitecture?

4. (15% total) In Table 2, we have given you four different sequences of addresses generated by a program running on a processor with a data cache. Cache hit ratio for each sequence is also shown in Table 2. Assuming that the cache is initially empty at the beginning of each sequence, find out the following parameters of the processors' data cache:

4.1 (3%) Associativity? (1, 2, or 4 ways)

4.2 (4%) Block size? (1, 2, 4, 8, 16, or 32 bytes)

4.3 (4%) Total cache size? (256 bytes, or 512 bytes)

4.4 (4%) Replacement policy? (LRU, or FIFO)

Table 2.

Sequence No.	Address Sequence	Hit Ratio
1	0, 2, 4, 8, 16, 32	0.33
2	0, 512, 1024, 1536, 2048, 1536, 1024, 512, 0	0.33
3	0, 64, 128, 256, 512, 256, 128, 64, 0	0.33
4	0, 512, 1024, 0, 1536, 0, 2048, 512	0.25

國立中山大學107學年度碩士暨碩士專班招生考試試題

科目名稱：計算機結構【資工系碩士班甲組、乙組】　　題號：434001

※本科目依簡章規定「不可以」使用計算機(問答申論題)　　

5. (10% total) Please answer the following questions:

5.1 (6%) Suppose you would like to connect 625 processors, and you are considering three different topologies: bus, point-to-point network, and mesh. Describe one disadvantage of each : (i) A single Bus(2%) (ii) A point-to-point network(2%) (iii) A 25×25 Mesh(2%).

5.2 (4%) Which one of these three topologies would you choose to connect 625 processors? Why?

6. (15% total) The Tomasulo's algorithm requires tag broadcast and comparison to enable wake-up of dependent instructions. To implement Tomasulo's algorithm in a machine that has the following properties:

- 8 functional units where each functional unit has a dedicated separate tag and data broadcast bus.
- 32 64-bit architectural registers.
- 16 reservation station entries per functional unit.
- Each reservation station entry can have two source registers.

6.1 (3%) What is the number of tag comparators per reservation station entry?

6.2 (3%) What is the total number of tag comparators in the entire machine?

6.3 (3%) What is the (minimum possible) size of the tag?

6.4 (3%) What is the (minimum possible) size of the register alias table (or, frontend register file) in bits?

6.5 (3%) What is the total (minimum possible) size of the tag storage in the entire machine in bits?

7. (10% total) You are requested to parallelize an old program so that it could run faster on modern multicore processors. Please answer the following questions.

7.1 (5%) If your program can perform 90% of its work (measured as processor-seconds) in the parallel portion and 10% of its work in the serial portion. The parallel portion is perfectly parallelizable. What is the maximum speedup of the program if the multicore processor had an infinite number of cores?

7.2 (5%) How many processors would be required to attain a speedup of 4?

8. (15% total) A memory system is configured as:

- There are two DRAM channels.
- Each channel has two ranks of DRAM chips.
- Each memory channel is controlled by a separate memory controller.
- Each rank of DRAM contains eight banks.
- Each bank contains 32K rows.
- Each row in one bank is 8KB.

Assume the minimum retention time among all DRAM rows in the system is 64 ms. In order to ensure that no data is lost, every DRAM row is refreshed once per 64 ms. Every DRAM row refresh is initiated by a command from memory controller which occupies the command bus on the associated memory channel. Consider a 1.024 second span of time.

Define the *utilization* (of a resource such as a bus or a memory bank) as the fraction of total time for which a resource is occupied by a refresh command.

For each calculation in this question, you may leave your answer in simplified form in terms of powers of 2 and powers of 10.

8.1 (4%) How long does each refresh command occupy the command bus (in ns) such that across all memory channels, the command bus utilization due to refreshes is 8.192%? (Hint $8.192 = 2^{13}/1000$)

8.2 (4%) How long does each refresh command occupy the DRAM banks (in ns) such that across all the banks, the banks utilization due to refreshes is 8.192%?

8.3 (3%) What data bus utilization, across all memory channels, is directly caused by DRAM refreshes?

8.4 (4%) How many refreshes are performed by the memory controllers during the 1.024 second period in total across both memory channels combined?

國立中山大學107學年度碩士暨碩士專班招生考試試題

科目名稱：工程數學【資工系碩士班乙組】　　題號：434002

※本科目依簡章規定「不可以」使用計算機(問答申論題)　　

1. (20%) The Laplace Transform of $f(t)$ is $F(s)$ (*i.e.*, $L[f(t)] = F(s)$). Assume that

$$f(t) = \frac{3}{4}(\sin 4t)(e^{-5t} - e^{2t}) + (2t^2 - 7t)H(t-3)e^{2t}\delta(t) .$$

When s = 3,

$$L\left[\int_0^t f(k)dk\right] = \square\ln 2/\square 4 + \square e^{\square}$$

Please find A+B+C+D = ?

《Hint: $L[tf(t)] \cdot L[\frac{1}{t}g(t)] = L[f(t)g(t)]$ 》

2. (10%) Given one logical circuit (as shown in Figure 1) and the corresponding truth table is provided in Table 1 as well. We assume the initial state of *clk* signal is 1. In addition, one value will be assigned to input *D* every one clock cycle. The output of this circuit is *Q* and *Q'* and the input sequence of *D* input is

1　0　1　1　0　0　1　0

Please find the Laplace transforming results of output *Q*.

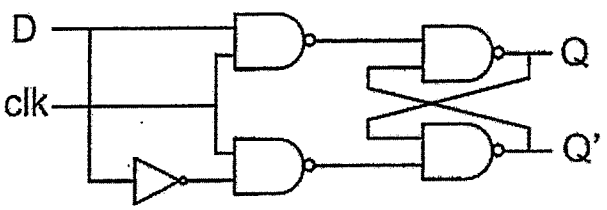

Figure 1.

Table 1.

Input Signal		Output Signal	
clk	D	Q	Q'
0	0	Q	Q'
0	1	Q	Q'
1	0	0	1
1	1	1	0

3. (10%) One differential equation $y'' + 3y' + 2y = 3e^{-t}$ as $y(0) = 0$ and $y'(0) = 1$.

3.1 (5%) Please solve the initial value problems.

3.2 (5%) Please verify your answer by using Laplace transformation.

4. (20%) Please find the Fourier series of the function $f(x) = \cos^3 2x + \sin^5 x$.

5. (30%) Let matrix $A = \begin{bmatrix} 3 & 1 & 1 \\ 2 & 4 & 2 \\ -1 & -1 & 1 \end{bmatrix}$.

5.1 (10%) Please find the eigenvalues and the corresponding eigenvector of the matrix *A*.

5.2 (10%) Find matrix *P* that makes matrix *A* diagonal.

5.3 (10%) Are the A^T and A^{-1} both dragonized as well? If yes, please prove your reason.

6. (10%) Let matrix $A = \begin{bmatrix} 1 & 1 \\ 1 & 1 \\ 0 & 0 \end{bmatrix}$. Please decompose the *A* by using SVD decomposition.

試題隨卷繳回

國立中山大學107學年度碩士暨碩士專班招生考試試題

科目名稱：作業系統與資料結構【資工系碩士班甲組】　　題號：434003

※本科目依簡章規定「不可以」使用計算機(問答申論題)　　

1. [Process Management: 15%]

(1) Explain the two basic models of inter-process communication. (4%)
(2) When will a race condition occur? (2%)
(3) What are the three requirements that a critical-section solution should meet? (3%)
(4) What is the difference between deadlock prevention and deadlock avoidance? (4%)
(5) When will priority inversion occur in process synchronization? (2%)

2. [Memory Management: 15%]

(1) What device deals with address translation? In which case we will not use this device? (3%)
(2) Please give two benefits of using paging. (4%)
(3) Does any system use the optimal page replacement method? Why or why not? (2%)
(4) Let average page-fault time and memory-access time be 70μs and 250ns, respectively. What is the expected page-fault rate if we want to get effective access time smaller than 285ns? List your calculation. (4%)
(5) What is reentrant code? (2%)

3. [Storage and I/O Management: 15%]

(1) When a file is opened, what are the four items of file information kept in UNIX? (4%)
(2) Consider a disk queue with requests for I/O to blocks on cylinders 100, 185, 40, 120, 2, 138, 75 and 87. Let the disk head currently stay at cylinder 60, and the maximum cylinder be 200. Please give the results of SSTF and C-LOOK scheduling methods. (6%)
(3) How does the parity bit work in RAID? (2%)
(4) Give three methods for CPU to know whether data are ready in an I/O device. (3%)

4. [Protection and Security: 15%]

(1) What is the principle of least privilege? How does Sun Microsystems OS implement it? (4%)
(2) Why language-based protection may not be secure? (3%)
(3) How do polymorphic and tunneling viruses bypass the detection of antivirus software? (4%)
(4) How does the digital-signature algorithm work? (2%)
(5) How does DDoS work? (2%)

5. [Basic Data Structures: 15%]

(1) Consider a binary tree. Suppose that its DFS result is "c, b, e, f, d, h, i, g, k, a, j" while BFS result is "c, b, g, e, d, k, j, f, h, i, a". Please draw the tree. (3%)
(2) Given the postfix of an equation "2 4 + 6 × 9 8 − 3 5 + × −", please compute its result. List your calculation. (3%)
(3) What is a binary search tree? Explain its property. (2%)
(4) Except that every node is either red or black, how can you make a binary search tree become a red-black tree? (4%)
(5) Show that the worst-case complexity of quicksort is $O(n^2)$. (3%)

6. [Advanced Data Structures: 15%]

(1) Given an n-key B-tree with minimum degree t, what is the upper bound of tree height? Prove the correctness of your answer. (8%)
(2) What is a B*-tree? (2%)
(3) Given a binomial tree B_k, show that there are exactly $C(k, i)$ nodes at depth i, where $C(k, i)$ denotes a combination function. (5%)

7. **[True/False Question: 10%]** Please mark 'O' or 'X' to answer each question.
   (1) The average-case time complexity of selection sort is O(n lg$n$). (1%)
   (2) LIFO and FIFO policies can be implemented by queues and stacks, respectively. (1%)
   (3) A hash has no inverse functions. (1%)
   (4) A red-black tree with k internal nodes has height no more than 2lg(k-1). (1%)
   (5) A tree contains no cycles. (1%)
   (6) Threads in the same process can directly share memory and common variables. (1%)
   (7) In any case, a user process is prohibited to use kernel data structures. (1%)
   (8) A hard real-time OS can be implemented by preemptive, priority-based scheduling. (1%)
   (9) The wait-die scheme is a preemptive-based solution for deadlock prevention. (1%)
   (10) Write-through policy is more reliable than write-back policy for caches. (1%)

國立中山大學 107 學年度碩士暨碩士專班招生考試試題

科目名稱：離散數學【資工系碩士班甲組】　　題號：434004

※本科目依簡章規定「不可以」使用計算機(問答申論題)　　

There are 6 problems in this test. Note that you should write down detailed steps for the solution to each problem; otherwise, no credits for that problem will be given.

1. Find the coefficient of x^7 in each of the following formulas.
   (a) [10%] $((x^2-3x)/(1-x)^5)+3x^7+5$.
   (b) [10%] $-2/((x-1)(x-2))$.

2. Consider the counting of the number of onto functions $H: A \to B$ where $|A| \geq |B|$.
   (a) [10%] Find the exponential generating function for the above counting such that the coefficient of $\frac{x^{|A|+2}}{|A|!}$ is the answer of the above counting.
   (b) [10%] Apply the above exponential generating function to find the answer of the above counting where $|A| = 10$ and $|B| = 3$.

3. Let $\Sigma = \{0, 1\}$ be an alphabet and $A = \{1, 00, 10\}$ be a subset of Σ^*.
   (a) [10%] For each integer $n \geq 1$, let a_n be the number of strings in A^* of length n. Find and solve a recurrence relation for a_n.
   (b) [10%] For each integer $n \geq 1$, let b_n be the number of strings in A^* which are of length n and exactly divided by 2 when we regard each of the strings as a binary number. Find b_n.

4. Consider the additive group $(\mathbf{Z}_8, +)$.
   (a) [5%] What is the order of 6? Why?
   (b) [5%] Find all generators of the group.

5. Consider the multiplicative group $(\mathbf{Z}^*_{196}, \cdot)$.
   (a) [5%] What is the order of the group? Why?
   (b) [5%] Find the inverse of 25.

6. Let $(\mathbf{Z}\times\mathbf{Z}, \oplus)$ be the group with $(a, b)\oplus(c, d) = (a+c+2, b+d-2)$ for any $(a, b), (c, d) \in \mathbf{Z}\times\mathbf{Z}$ where $a+c+2$ and $b+d-2$ are computed using ordinary addition and subtraction in $\mathbf{Z}$.
   (a) [2%] $3(4, 5) = (4, 5)\oplus(4, 5)\oplus(4, 5) = ?$
   (b) [5%] What is the identity of the group?
   (c) [5%] What is the inverse of (a, b)?
   (d) [8%] Let $(\mathbf{G}, +)$ be an additive group and let $h: \mathbf{Z}\times\mathbf{Z} \to \mathbf{G}$ be a group homomorphism where $h(3, 2) = u$ and $h(-2, 6) = v$. Please express $h(18, 22)$ in terms of u and v.

試題隨卷繳回