國立中山大學115學年度
碩士班考試入學招生考試試題

科目名稱：電子學(含數位電路)【IC設計領域聯招碩士班、電機系碩士班己組、IC設計所碩士班】

－作答注意事項－

考試時間：100分鐘

- **考試開始鈴響前不得翻閱試題，並不得書寫、劃記、作答。**請先檢查答案卷（卡）之應考證號碼、桌角號碼、應試科目是否正確，如有不同立即請監試人員處理。
- **答案卷限用藍、黑色筆(含鉛筆)書寫、繪圖或標示**，可攜帶橡皮擦、無色透明無文字墊板、尺規、修正液（帶）、手錶(未附計算器者)。每人每節限使用一份答案卷，請衡酌作答。
- 答案卡請以2B鉛筆劃記，不可使用修正液（帶）塗改，未使用2B鉛筆、劃記太輕或污損致光學閱讀機無法辨識答案者，後果由考生自負。
- 答案卷（卡）應保持清潔完整，不得折疊、破壞或塗改應考證號碼及條碼，亦不得書寫考生姓名、應考證號碼或與答案無關之任何文字或符號。
- 可否使用計算機請依試題資訊內標註為準，如「可以」使用，廠牌、功能不拘，唯不得攜帶書籍、紙張（應考證不得做計算紙書寫）、具有通訊、記憶、傳輸或收發等功能之相關電子產品或其他有礙試場安寧、考試公平之各類器材入場。
- **試題及答案卷（卡）請務必繳回，未繳回者該科成績以零分計算。**
- **試題採雙面列印，考生應注意試題頁數確實作答。**
- **違規者依本校招生考試試場規則及違規處理辦法處理。**

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※本科目依簡章規定「可以」使用計算機（廠牌、功能不拘）（混合題）

Part I. Multiple-choice questions (Single answer).
Only one option is correct for each question in this part.

1. (2%) Which component is the main contributor to power consumption in a CMOS circuit during normal operation?
   A. Static leakage power
   B. Dynamic switching power
   C. Short-circuit power only
   D. Gate-oxide tunneling power
2. (2%) If the supply voltage V_{DD} is reduced by 50%, how does dynamic power change (all other parameters constant)?
   A. Reduced by 50%
   B. Reduced by 75%
   C. Reduced by 40%
   D. Reduced by 25%
3. (2%) Why is static power consumption ideally very low in CMOS circuits?
   A. NMOS and PMOS are never ON
   B. There is no DC path between V_{DD} and GND in steady state
   C. CMOS circuits operate at low frequency
   D. CMOS transistors have zero resistance
4. (2%) Which technique is most effective for reducing both dynamic and static power in CMOS systems?
   A. Increasing transistor width
   B. Clock gating only
   C. Power gating idle blocks
   D. Increasing supply voltage
5. (2%) Lowering V_{DD} in a CMOS circuit generally leads to which trade-off?
   A. Lower power and higher speed
   B. Lower power and increased delay
   C. Higher noise margin and lower power
   D. No change in circuit behavior
6. (2%) In a 2-input CMOS NAND gate, how are the NMOS transistors connected?
   A. In parallel
   B. In series
   C. One in series, one in parallel
   D. Cross-coupled
7. (2%) Why are PMOS transistors typically sized wider than NMOS transistors in CMOS logic gates?
   A. PMOS has higher mobility
   B. NMOS has higher threshold voltage
   C. PMOS has lower carrier mobility
   D. PMOS must carry leakage current
8. (2%) Which logic function is most expensive to implement using static CMOS in terms of transistor count?
   A. NAND
   B. NOR
   C. XOR
   D. NOT

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9. (2%) What does propagation delay of a CMOS logic gate represent?
   A. Time for input voltage to change
   B. Time for output to reach 50% after an input transition
   C. Clock-to-output delay
   D. Setup time of a flip-flop
10. (2%) If the load capacitance of a CMOS gate doubles, the propagation delay will approximately:
   A. Remain unchanged
   B. Double
   C. Be reduced by half
   D. Increase logarithmically
11. (2%) Which design change most effectively reduces propagation delay?
   A. Increasing threshold voltage
   B. Increasing transistor width
   C. Lowering supply voltage
   D. Increasing logic depth
12. (2%) In a multi-stage CMOS logic path, total propagation delay is best approximated as:
   A. Maximum delay of any single gate
   B. Average delay of all gates
   C. Sum of delays of gates on the critical path
   D. Delay of the first gate only
13. (2%) Why do CMOS logic gates generally have larger noise margins than TTL gates?
   A. CMOS operates at higher frequency
   B. CMOS has lower threshold voltage
   C. CMOS has rail-to-rail output swing
   D. CMOS uses resistive pull-up networks
14. (2%) Which parameter directly affects the noise margin of a CMOS logic gate?
   A. Load capacitance
   B. Output resistance
   C. Input threshold voltages
   D. Switching frequency
15. (2%) Which design change most directly improves noise margin in a CMOS inverter?
   A. Increasing load capacitance
   B. Increasing transistor channel length
   C. Balancing PMOS and NMOS strengths
   D. Increasing switching frequency
16. (4%) Given the circuit in Fig. 1, transistors M_1 and M_2 have identical process parameters: $\mu_n C_{ox}(\frac{W}{L}) = 200\ \mu A/V^2$, $V_{th} = 0.7$ V, $\lambda = 0.01$. $R_S = 1\ k\Omega$, while V_1 and V_2 are DC bias voltages. Assume $I_0 = 400\ \mu A$, and both M_1 and M_2 operate in the saturation region. What is the value of V_1?
   A. 1.1 V
   B. 4.0 V
   C. 3.1 V
   D. 2.0 V
17. (4%) Based on Question 16, what is the minimum value of V_2?
   A. 5.1 V
   B. 3.1 V
   C. 2.7 V
   D. 4.4 V

18. (4%) Based on Question 16, which of the following is closest to the value of the small-signal output resistance R_o?
    A. 100 MΩ
    B. 10 MΩ
    C. 1 MΩ
    D. 100 kΩ

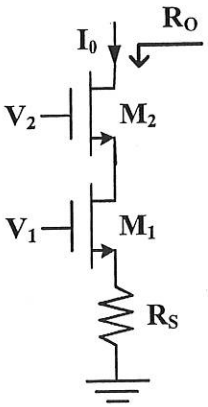

Fig. 1

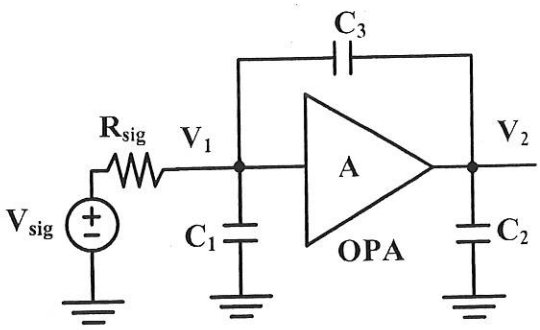

Fig. 2

19. (4%) In the circuit shown in Fig. 2, R_{sig} = 10 kΩ, C_1 = 0.1 pF, C_2 = 3 pF, C_3 = 1 pF, and the amplifier gain is A = −100. Assume the operational amplifier (OPA)'s input resistance is infinite. which of the following is closest to the value of the small-signal equivalent capacitance seen at node V_1?
    A. 0.1 pF
    B. 1 pF
    C. 4 pF
    D. 100 pF
20. (4%) Based on Question 19, which of the following is closest to the value of the small-signal equivalent capacitance at node V_2?
    A. 0.1 pF
    B. 1 pF
    C. 4 pF
    D. 100 pF
21. (4%) For an NMOS transistor, which of the following statements is correct?
    A. The gate capacitance is mainly determined by the channel width W.
    B. Reducing the drain current I_D can increase the voltage gain.
    C. Increasing the channel width W can increase the voltage gain.
    D. The small-signal impedance seen looking into the source terminal is r_o.
22. (4%) In the circuit shown in Fig. 3, the input voltage is V_I = 1.0 V and the output voltage is V_O = 0.99 V. What is the magnitude of the voltage gain of the operational amplifier (OPA)? Choose the closest value.
    A. The voltage gain is infinite.
    B. The voltage gain is 100.
    C. The voltage gain is 10.
    D. The voltage gain cannot be determined.

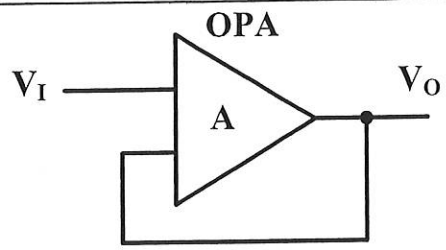

Fig. 3

23. (4%) Regarding a PN diode, which of the following statements is incorrect?
    A. As the forward bias voltage increases, the diffusion capacitance increases.
    B. The saturation current I_S of a PN diode increases as the temperature rises.
    C. The saturation current I_S is generally a constant and is independent of the junction area.
    D. Breakdown phenomena mainly occur in the depletion region.

Part II. Multiple-choice questions (Multiple answers).
Each question is worth points only if all correct answers are selected; otherwise, the question will receive zero points.

24. (2%) Which techniques can reduce static (leakage) power?
    A. Power gating
    B. High-threshold voltage transistors
    C. Clock gating
    D. Lowering temperature
25. (2%) Which statements about CMOS power scaling are correct?
    A. Dynamic power scales quadratically with V_{DD}
    B. Static power is independent of technology scaling
    C. Leakage power becomes dominant in advanced nodes
    D. Lowering V_{DD} always improves performance
26. (2%) Which statements about static CMOS logic gates are correct?
    A. They provide full rail-to-rail output swing
    B. They consume zero power during switching
    C. They have good noise margins
    D. They use complementary PMOS and NMOS networks
27. (2%) Which techniques improve performance of CMOS logic gates?
    A. Increasing transistor width
    B. Reducing load capacitance
    C. Lowering supply voltage
    D. Reducing logic depth
28. (2%) Which issues become more severe as CMOS logic gates scale to advanced technology nodes?
    A. Leakage current
    B. Process variation
    C. Noise margin
    D. Interconnect delay
29. (2%) Which factors increase the propagation delay of a CMOS logic gate?
    A. Larger load capacitance
    B. More transistors in series
    C. Higher supply voltage
    D. Smaller transistor width
30. (2%) Which statements about CMOS propagation delay are correct?

A. Delay limits maximum clock frequency
B. Delay is independent of temperature
C. Higher temperature increases delay
D. Delay affects setup time constraints

31. (2%) Which statements about CMOS noise margin are correct?
A. Larger noise margin improves reliability
B. Noise margin depends on load capacitance
C. Noise margin can be obtained from the VTC
D. Noise margin affects tolerance to interference

32. (2%) Which issues become more critical for noise margin in advanced CMOS technologies?
A. Reduced supply voltage
B. Increased process variation
C. Improved output swing
D. Device mismatch

33. (2%) Which statements regarding noise margin and system design are correct?
A. Noise margin affects timing only
B. Noise margin impacts functional correctness
C. Larger noise margin improves tolerance to crosstalk
D. Noise margin is unrelated to reliability

Part III. Essay Questions
You must show all calculation and derivation steps for each question. Answers without supporting work may receive zero points.

34. (9%) The op amp (OPA) in the circuit of Fig. 4 has an open-loop gain of 10^5 and a single-pole rolloff with $\omega_{3dB} = 10$ rad/s.
(a) Sketch a Bode plot for the loop gain. (3%)
(b) Find the frequency at which $|A\beta| = 1$, and find the corresponding phase margin. (3%)
(c) Find the closed-loop transfer function, including its zero and poles. (3%)

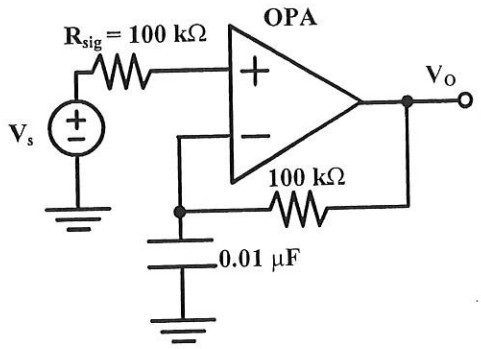

Fig. 4

35. (9%) Fig. 5 shows a circuit suitable for op-amp applications. For all transistors $\beta = 100$, $V_{BE} = 0.7\,V$, and $r_o = \infty$.
(a) For inputs grounded and output held at 0 V (by negative feedback) find the collector currents of all transistors. (3%)
(b) Calculate the gain of the amplifier with a load of 10 kΩ. (3%)
(c) With loads as in (b) calculate the value of the capacitor C_1 required for a 3-dB frequency of 1 KHz. (3%)

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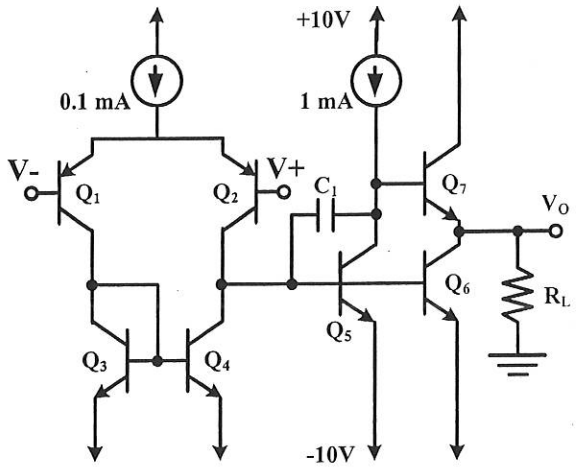

Fig. 5