國立中山大學113學年度
碩士班暨碩士在職專班招生考試試題

科目名稱：電子學【IC設計所碩士班】

—作答注意事項—

考試時間：100分鐘

- **考試開始鈴響前不得翻閱試題，並不得書寫、劃記、作答。**請先檢查答案卷（卡）之應考證號碼、桌角號碼、應試科目是否正確，如有不同立即請監試人員處理。
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國立中山大學 113 學年度碩士班暨碩士在職專班招生考試試題

科目名稱：電子學【IC 設計所碩士班】　　題號：483002

※本科目依簡章規定「可以」使用計算機（廠牌、功能不拘）（問答申論題）　　

[Problem 1] **(20%)** For the circuit shown in Fig. 1, let $\beta = 125$, $V_{BE(on)} = 0.7$ V, and $V_A = 200$ V.

(a) Plot the dc and ac load lines on the same graph. (10%)

(b) Determine the maximum symmetrical swing in the output voltage for $i_C > 0$ and $0.5 \le v_{CE} \le 9.5$ V. (10%)

Please note that you need to show how you derive the results.

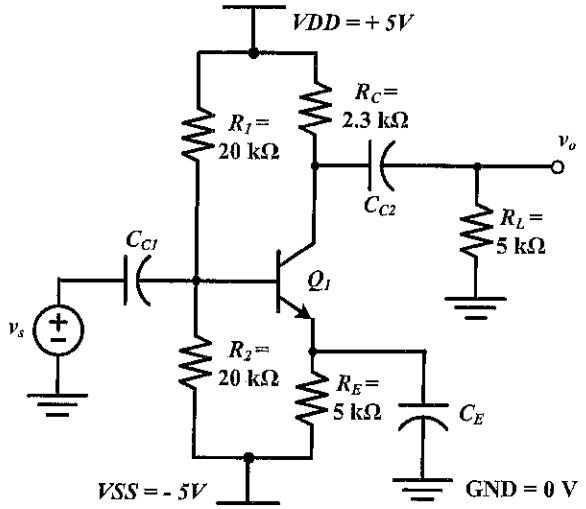

Fig 1

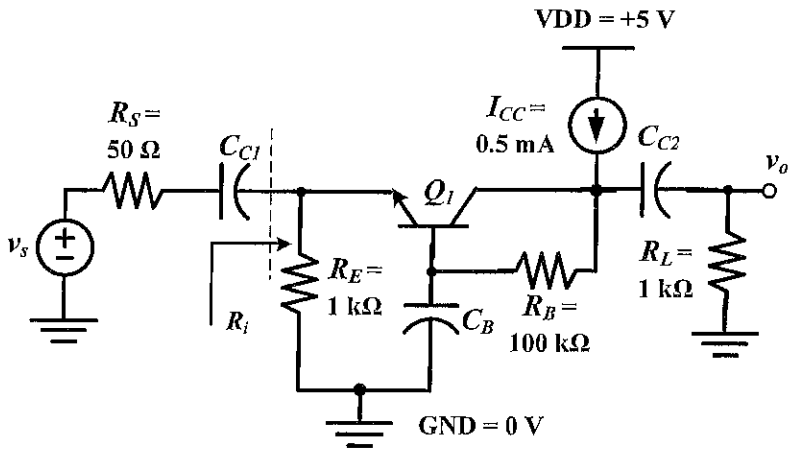

Fig. 2

[Problem 2] **(19%)** For the circuit shown in Fig. 2, the transistor parameters are β =100 and $V_A = \infty$.

(a) Determine the dc voltages at the collector, base, and emitter terminals. (9%)

(b) Determine the small-signal voltage Av = v_o/v_s. (5%)

(c) Find the small-signal input resistance R_i. (5%)

[Problem 3] **(14%)** A three-pole feedback amplifier has a loop gain given by

$$T(f) = \frac{\beta(10^5)}{\left(1 + j\frac{f}{5 \times 10^2}\right)\left(1 + j\frac{f}{10^4}\right)^2}$$

(a) Determine the frequency f_{180} at which the phase is -180 degrees. (7%)

(b) At the frequency f_{180}, determine the value of β such that $|T(f)| = 1$. (7%)

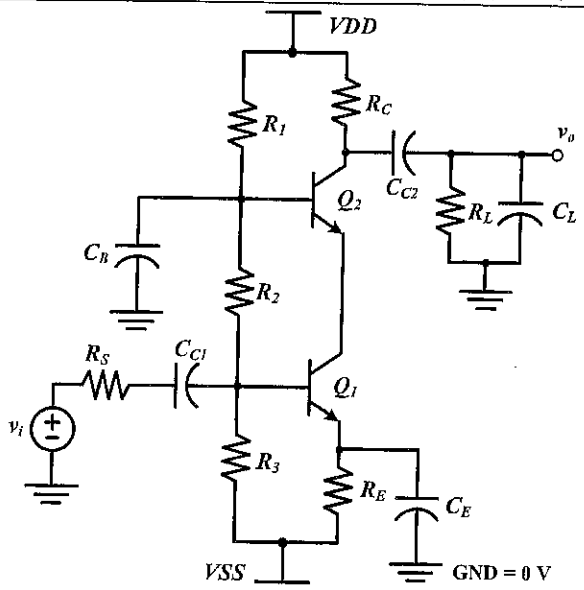

Fig. 3

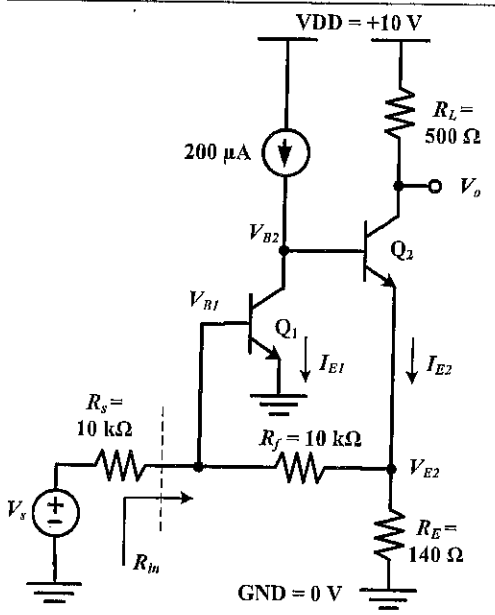

Fig. 4

[Problem 4] **(21%)** For the cascode circuit shown in Fig. 3, the circuit parameters are VDD = 10 V, VSS = -10 V, R_S = 0.1 kΩ, R_1 = 42.5 kΩ, R_2 = 20.5 kΩ, R_3 = 28.3 kΩ, R_E = 5.4 kΩ, R_C = 5 kΩ, R_L = 10 kΩ, C_L = 0. The transistor parameters are β_O = 120, $V_A = \infty$, $V_{BE(on)}$ = 0.7 V, C_π = 12 pF and C_μ = 2 pF.

(a) If C_L is an open circuit, determine the 3 dB frequency corresponding to the input and output portions of the equivalent small-signal circuit. (12%)

(b) Determine the midband voltage gain. (6%)

(c) If a load capacitor C_L = 50 pF is connected to the output, determine if the upper 3 dB frequency is dominated by the load capacitance or by the transistor characteristics. (3%)

[Problem 5] **(26%)** For the amplifier circuit in Fig. 4, assuming that $V_{BE(on)}$ = 0.7 V, β =100, and V_s has a zero dc component, answer the following questions.

(a) Find the dc voltages at all nodes (V_{B1}, V_{B2}, V_{E2}, and V_o) and the dc emitter currents of Q1 and Q2 (I_{E1}, and I_{E2}). (18%)

(b) Use feedback analysis to find V_o/V_s and R_{in}. (8%)

國立中山大學113學年度
碩士班暨碩士在職專班招生考試試題

科目名稱：數位系統設計【IC設計所碩士班】

—作答注意事項—

考試時間：100分鐘

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國立中山大學113學年度碩士班暨碩士在職專班招生考試試題

科目名稱：數位系統設計【IC設計所碩士班】　　題號：483001

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[Problem 1] **(20%)** Implement the following Boolean function

$F(w, x, y, z) = xy + w'x'z' + wx'y'z' + wx'yz.$

(a) by using only NOR gates. (5%)
(b) by using only NAND gates. (5%)
(c) by using the simplest sum-of-products form (5%)
(d) by drawing the logic diagram using a multiplexer (5%)

Please note that for (a), (b) and (c) you need to show the final Boolean function and how you derive the function.

[Problem 2] **(12%)** Short answer questions:

(a) Provide an example to demonstrate that a Boolean function can have more than one simplest form of expression, indicating its non-uniqueness. (3%)
(b) Provide an overview of the hardware structure of a sequential circuit and utilize this structure to explain how a sequential circuit is different in functionality and design from a combinational circuit. (4%)
(c) Present several waveform diagrams to illustrate and clarify the concepts of setup time and hold time in a D flip-flop. (5%)

[Problem 3] **(18%)** Design an asynchronously resettable positive edge-triggered finite state machine that accepts a one-bit input d and generates two one-bit outputs x and y. x should be 1 if d has been 0 for at least two consecutive cycles. y should be 1 if d has been 0 for at least three cycles (not necessarily consecutively).

(a) Give Verilog/VHDL codes of an asynchronously resettable positive edge-triggered flip-flop. (3%)
(b) Draw the state transition diagram and define each state clearly. (5%)
(c) Write RTL Verilog/VHDL codes to implement the finite state machine you designed in (b). (10%)

[Problem 4] **(20%)** (a) Assume that the 4-bit binary adders are available. Please design a combinational circuit for the addition of two BCD digits using the 4-bit binary adder. Please draw the final logic circuit of the BCD adder with the 4-bit binary adder circuit block. Please note that you don't have to show the details of the 4-bit binary adder. (10%) (b) Design a combinational circuit that generates the 9's complement of a BCD digit. Please note that you need to show the final Boolean function and how you derive the function. (10%)

[Problem 5] **(15%)** (a) Design a counter with T flip-flops that goes through the following binary repeated sequence: 0, 1, 3, 7, 6, 4. Show that when binary states 010 and 101 are considered as don't care conditions, the counter may not operate properly.(10%) (b) Find a way to correct the design. (5%) Please note that you need to show the final Boolean function, the state diagram and how you derive the function.

[Problem 6] **(15%)** A circuit for a gated D-latch is shown in Fig. 1. Assume that the propagation delay through a NAND gate or an inverter is 1 ns. Complete the timing diagram given in the Fig. 2, which shows the signal values with 1 ns resolution. Please note that you need to redraw the timing diagram in your answer sheet.

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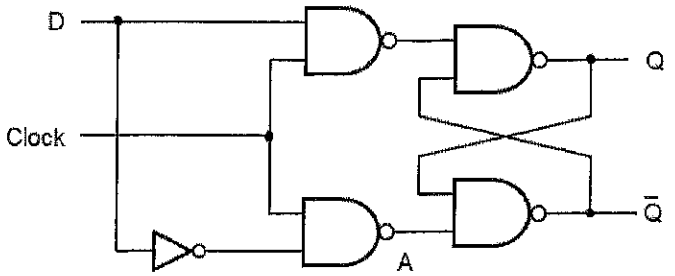

Fig. 1

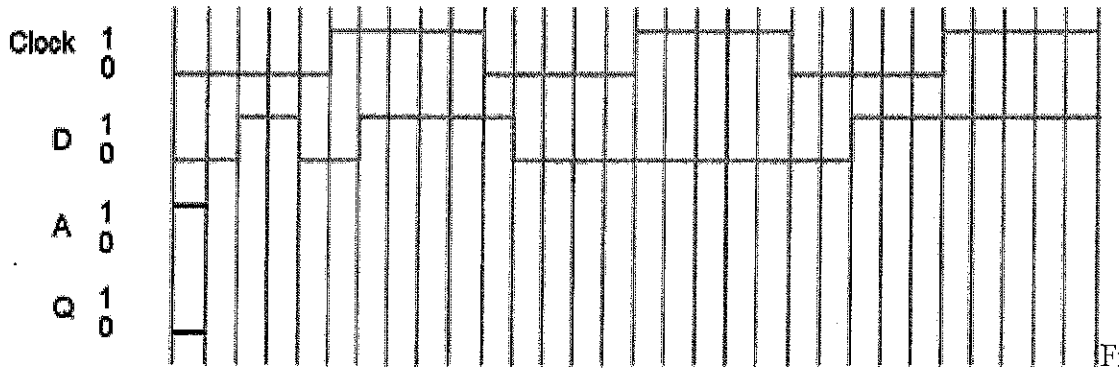

Fig. 2